

REMARKS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

The Examiner objected to claims 1 and 2 due to informalities. Applicant notes that claim 1 has been amended to overcome the objection.

The Examiner rejected claims 1 and 2 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant notes that claims 1 and 2 have been amended to overcome the 35 U.S.C. 112, second paragraph rejection.

The Examiner rejected claims 1 and 2 under 35 U.S.C. 103(a) as being unpatentable over Chiu et al., U.S. Pat. Pub. No. 2004/0118501 in view of Applicant's admitted prior art ("AAPA"). The Examiner's rejection is traversed for the following reason.

Applicant discloses a module structure for a semiconductor device. The module structure includes a high-resistance layer of a first conductive type, a base layer of a second conductive type formed in an upper part of the high-resistance layer, an emitter region of a first conductive type formed in an upper part of the base layer, whereby the emitter region includes an emitter electrode. An insulated gate electrode is located adjacent to the base layer. The module structure further includes a guard ring part, wherein a portion of the guard ring extends deeper

toward a cell region, which includes the emitter region. A passivation layer is formed on an upper part of the guard ring part. The passivation layer does not extend into an upper part of the cell region. A buffer layer of a first conductive type is formed on an underside of the high-resistance layer and a collector layer of the second conductive type is formed on an underside of the buffer layer. A collector electrode connected to the collector layer. One end of a metal flat plate, which is an upper heat-sinking part, is connected to the emitter electrode at a height such that metal flat plate does not contact the passivation film of the semiconductor element. Thus, a gap exists between the semiconductor element or more specifically the passivation film and the heat-sinking part. The gap allows for thermal expansion of both the upper heat-sinking part and the passivation film thereby eliminating thermal stresses between layers in the semiconductor element.

Chiu discloses a heat transfer composite, which includes multiple heat transfer structures, for use in an integrated circuit (IC) die. The heat transfer composite is used to provide an interface subsystem between the IC die and a thermal management device, such as a heat spreader, to effectively transfer the heat generated by the IC to the thermal management device. Accordingly, Chiu does not teach all the features, for which it is cited, of claim 1. More specifically, Chiu does not teach “a metal flat plate upper heat-sinking part connected to the emitter electrode at a height such that it is non-contacting with the passivation film.”

Rather, Chiu teaches an IC die 418 having an active surface 420 and a backside surface 422 whereby the active surface 42 is mounted to a substrate 426, such as a printed circuit board. The backside surface 422 of the die 418 is connected to a thermal management device, such as a heat spreader 424, via an

interface subsystem 411. The interface subsystem 411, which is in the form of a heat transfer composite, is designed to effectively transfer the heat generated by the IC die 418 to the heat spreader 424. The heat spreader 424 is attached to the backside surface 422 of the die 418, such that there is no gap between the IC die 418 and the heat spreader 424, as required by claim 1 of the present invention. In addition, each end or lip 430 of the heat spreader 424 is also attached to the substrate 426 with a bonding material 428. Thus, Chiu does not teach a gap between an IC element and an upper heat sink to allow for thermal expansion.

In regard to AAPA, the Examiner did not cite AAPA as teaching an upper heat sink thereby admitting that AAPA does not teach an upper heat sink.

Based on the foregoing, it is apparent that Chiu, AAPA or the combination thereof do not teach all the features of claim 1. Thus, reconsideration and withdrawal of the rejections of claim 1 based upon Chiu and AAPA is hereby requested.

Claim 2 depends from claim 1, thus, all arguments pertaining to claim 1 are equally applicable to claim 2 and are herein incorporated by reference.

Regarding new claim 3, Chiu, AAPA or the combination thereof do not teach all the features of claim 3. More specifically, Chiu, AAPA or the combination thereof do not teach “wherein one end of the metal flat plate upper heat-sinking part is connected to the emitter electrode and the opposite end of the metal flat plate heat-sinking part is connected to a substrate.”

As explained above, both ends or lips 430 of the heat spreader 424 disclosed in Chiu are attached to the substrate 426. Thus, Chiu teaches attaching both ends of a heat spreader or heat sink to the substrate whereas in the present invention

only one end is connected to the substrate. Regarding AAPA, AAPA does not disclose an upper heat sink. Therefore, Chiu, AAPA or the combination thereof do not teach all the features of claim 3

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. SHM-16693.

Respectfully submitted,

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